

Figure 1

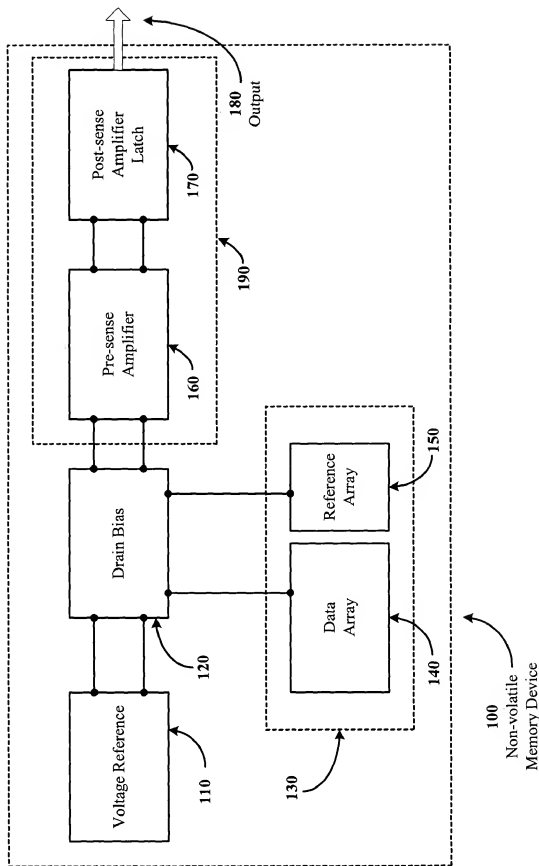
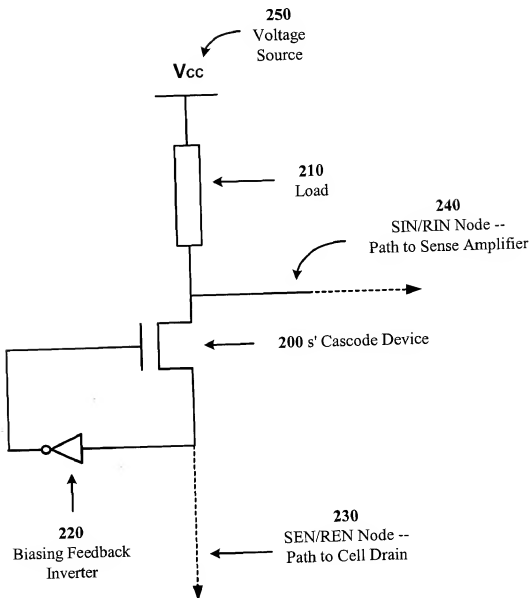
Flash Memory Sensing
Block Diagram

Figure 2

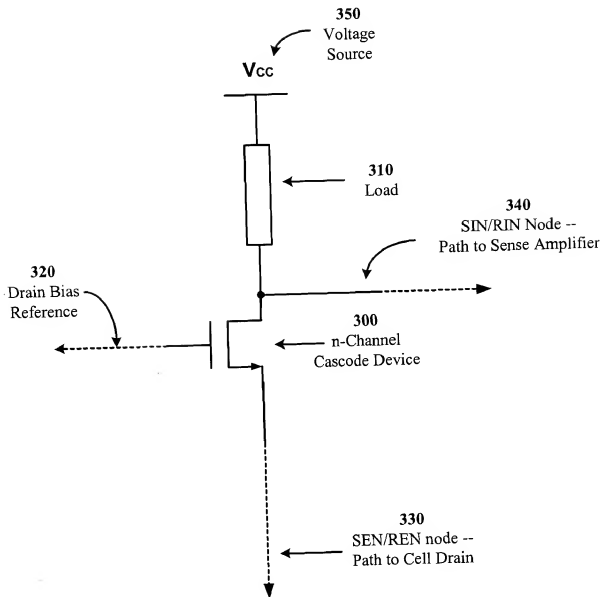
Conventional Feedback Drain Bias Circuit



006221-05525760

Figure 3

Static Reference
Drain
Bias Circuit



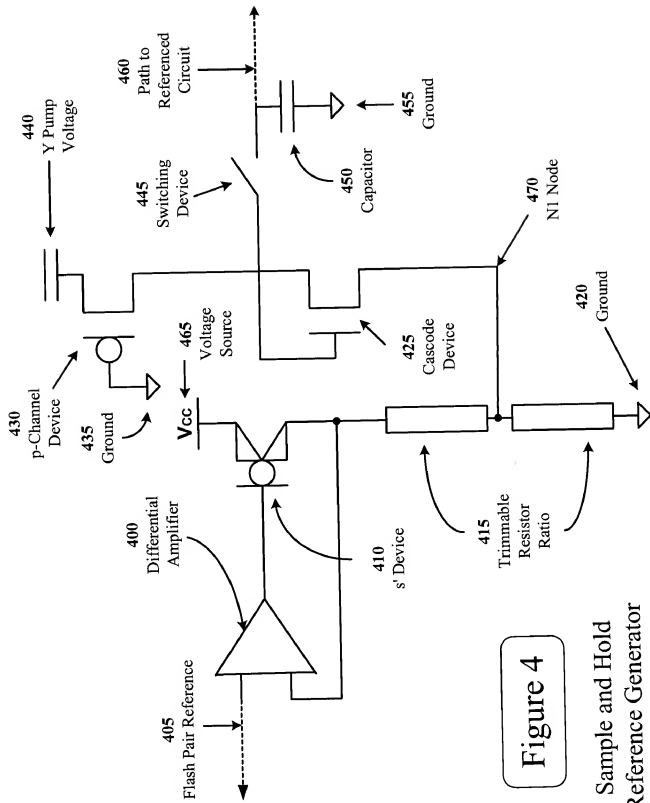


Figure 4

Sample and Hold
Reference Generator

Drain Bias
Current Mirror and
Column Load with
Sample and Hold
Reference

Figure 5

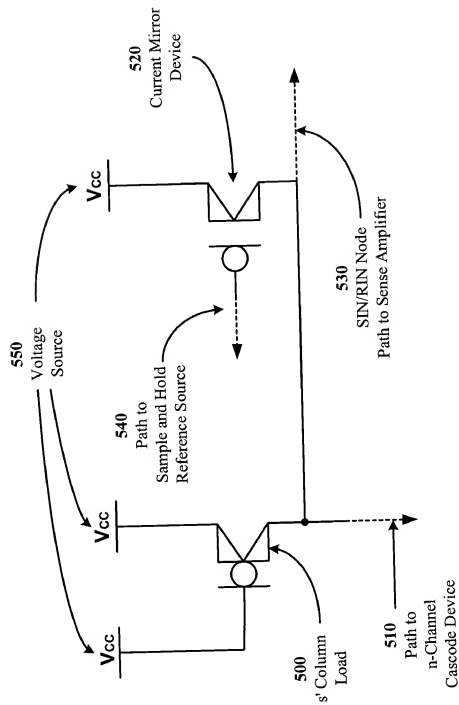


Figure 6

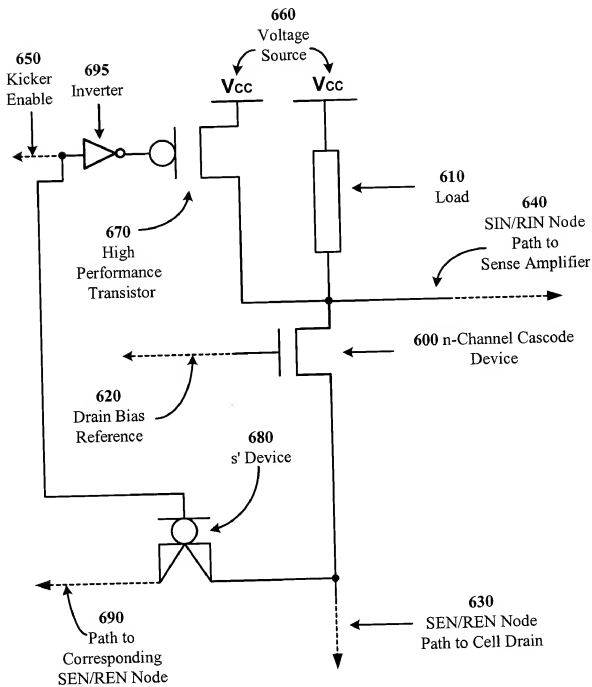
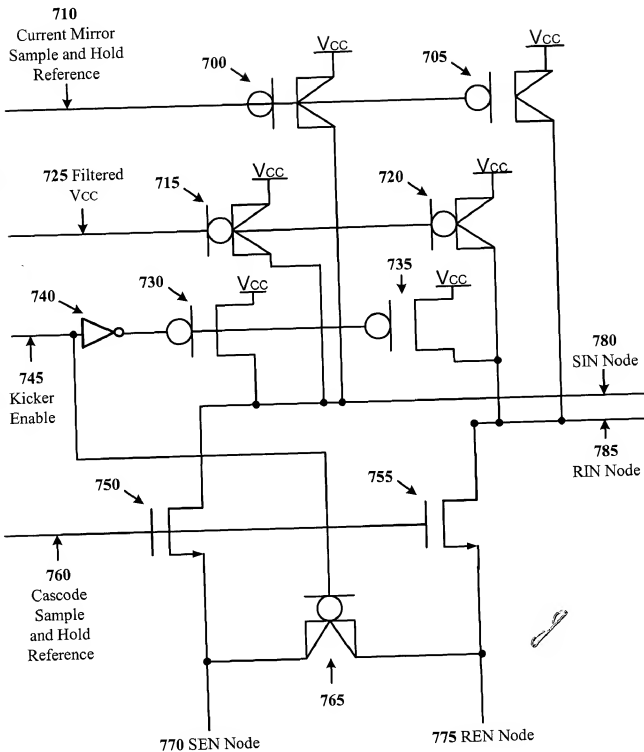
Drain Bias
Kicker Circuit

Figure 7

Drain Bias Pair Circuit Diagram



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